

Appl. No. 10/023,121; Docket No. NL 000723
Amdt. dated: November 10, 2005
Response to Office Action of October 4, 2005

Amendments to the Claims

1. *(Currently Amended)* An information processing system comprising a sender, a receiver and a communication channel coupled between the sender and the receiver, the communication channel being capable of transmitting time-continuously a first binary logic signal and second binary logic signal from the sender to the receiver, the sender being arranged to receive a succession of data values and information distinguishing successive clock phases, the sender being arranged to encode the data values and the information into a combination of the first signal and second signal, the sender using alternately a first and a second data dependent criterion to select which one of the first signal and second signal has a logic level change between immediately successive clock phases, so that the first signal and second signal are alternately mutually opposite and mutually equal, the first criterion selecting the level of the first signal dependent on the data value, the second criterion providing a level change of either the first signal or the second signal dependent on the data value.

2. *(Currently Amended)* An information processing system according to Claim 1, wherein the first signal and second signal for respective ones of the clock phases alternately depend on the data value for the clock phase according to the first criterion and on a change in the data values between the clock phase and an immediately neighboring clock phase according to the second criterion.

3. *(Original)* An information processing system according to Claim 1, wherein the first criterion is used in even clock phases and the second criterion is used in odd clock phases.

4. *(Currently Amended)* A sender circuit with a data producing circuit, a clock circuit, an encoder and a connection for a communication channel, ~~the producing~~ the data producing circuit being arranged to produce a succession of data values, the clock circuit being arranged to generate information distinguishing successive clock phases, encoder being arranged to encode the data values and the information into a combination of a first binary logic signal and second binary logic signal for time continuous transmission via the communication channel, the encoder using alternately a first and a second data dependent

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criterion to select which one of the first signal and second signal has a logic level change between immediately successive clock phases, so that the first signal and second signal are alternately mutually opposite and mutually equal, the first criterion selecting the level of the first signal dependent on the data value, the second criterion providing a level change of either the first signal or the second signal dependent on the data value.

5. (*Currently Amended*) A receiver circuit with a connection for a communication channel the receiver comprising an decoder and a data consuming circuit and connections for a communication channel, the decoder being arranged to recover a clock signal for data consuming circuit, the clock signal having a level change each time at least one of a first and second, time continuous binary logic signal on the connections undergoes a binary level change, the encoder being is arranged to decode ~~the data values~~ data values or successive clock phases of the clock signal using alternately a first and a second signal dependent criterion, the first criterion providing mutually opposite data values dependent on the level of the first signal, the second criterion providing mutually opposite data values dependent on whether the first signal or the second signal changes level between the clock phases.

6. (*Currently Amended*) Method of transmitting data and clock information in the form of a first and second time-continuous electric ~~binary logic signal~~, binary logic signals, wherein alternately a first and a second data dependent criterion is used to select which one of the first and second signal has a logic level change between immediately successive clock phases, so that the first signal and second signal are alternately mutually opposite and mutually equal, the first criterion selecting the level of the first signal dependent on ~~the data value~~, a data value, the second criterion providing a level change of either the first or the second signal dependent on the data value.